SESSION 26 – TAPA III
Emerging Non-Volatile Memories

Saturday, June 19, 10:20 a.m.
Chairpersons: H. McAdams, Texas Instruments
T. Kawahara, Hitachi

26.1 — 10:20 a.m.

An 8Mb Demonstrator for High-Density 1.8V Phase-Change Memories, F. Bedeschi, C. Resta, O. Khouri, E. Buda, L. Costa, M. Ferraro, F. Pellizzer, F. Ottogalli, A. Pirovano, M. Tosi, R. Bez, R. Gastaldi and G. Casagrande, STMicroelectronics, Milan, Italy

An 8Mb Non-Volatile Memory Demonstrator incorporating a novel 0.32 um2 Phase-Change Memory cell using a Bipolar Junction Transistor as selector and integrated into a 3V 0.18 um CMOS technology is presented. Realistically large 4Mb tiles with a voltage regulation scheme that allows fast bitline precharge and sense, and an innovative approach that minimizes the array leakage are proposed. Cells distributions and first endurance measurements demonstrate the chip functionality and a good working window.

26.2 — 10:45 a.m.

High Density and Low Power Nonvolatile FeRAM with Non-Driven Plate and Selected Driven Bit-Line Scheme, H. Hirano, M. Sakagami, K. Yamaoka, T. Nakakuma, S. Iwanari, Y. Murakuki, T. Miki, Y. Gohou and E. Fujii, Matsushita Electric Industrial Co., Ltd., Kyoto, Japan

We have successfully developed high density and low power embedded 1Mbit FeRAM. Low operating voltage of 1.5V with ferroelectric capacitor which operates at 0.75V was realized by using technology of 1) non-driven plate scheme with a non-refresh operation and 2) selected driven bit-line scheme. The memory core size is reduced down to 54% and the power consumption is reduced to approximately one-fiftieth compared with those of the conventional scheme.

26.3 — 11:10 a.m.

A Voltage-Dependent Switching-Time (VDST) Model of Ferroelectric Capacitors for Low-Voltage FeRAM Circuits, J. Chow, A. Sheikholeslami, J.S. Cross* and S. Masui, University of Toronto, Toronto, Ontario, Canada, *Fujitsu Laboratories Limited, Japan

The time required to switch a ferroelectric capacitor from one binary state to the other is strongly related to the magnitude of the applied voltage, especially at voltages well below the power supply. This paper presents a Verilog-A model that accurately predicts the voltage-dependent switching dynamics of various FeRAM technologies. Spectre simulations of low-voltage FeRAM circuits implemented in a 0.35 μm CMOS/PZT test chip are in full agreement with our measurement results.

26.4 — 11:35 a.m.

A 1.2V 1Mbit Embedded MRAM Core with Folded Bit-Line Array Architecture, T. Tsuji, H. Tanizaki, M. Ishikawa, J. Otani, Y. Yamaguchi, S. Ueno, T. Oishi and H. Hidaka, Renesas Technology Corporation, Itami, Hyogo, Japan

A 1Mbit MRAM with a 0.81um2 1-Transistor 1-Magnetic Tunnel Junction (1Tr-1MTJ) cell using 0.13um 4LM logic technology has been produced. A folded-bitline sensing and common write word-line scheme with dummy row architecture achieves 100MHz random read cycle with n+ diffusion/Co-saliside read source lines. Employing a distributed gate voltage control scheme, high speed write current switching without write disturb by peak current even at 1.2V power supply is demonstrated.

26.5 — 12:00 p.m.

A 16Mb MRAM Featuring Bootstrapped Write Drivers, J. DeBrosse, C. Arndt*, C. Barwin, A. Bette*, D. Gogl*, E. Gow, H. Hoenigschmid*, S. Lammers*, M. Lamorey, Y. Lu**, T. Maffitt, K. Maloney, W. Obermeyer*, A. Sturm*, H. Viehmann*, D. Willmott, M. Wood, W. J. Gallagher**, G. Mueller*and * A.R. Sitaram*, IBM Microelectronics Division, *Infineon Technologies, **IBM TJ Watson Research Ctr., Essex Junction, VT

A 16Mb Magnetic Random Access Memory (MRAM) is demonstrated in 0.18um three-Cu-level CMOS with a three-level MRAM process adder. The chip, the highest density MRAM reported to date, utilizes a 1.42um2 1-Transistor1-Magnetic Tunnel Junction (1T1MTJ) cell, measures 79mm2 and features a x16 asynchronous SRAM-like interface. The paper describes the cell, architecture, and circuit techniques unique to multi-Mb MRAM design, including a novel bootstrapped write driver circuit. Hardware results are presented.